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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,466	02/28/2002	Hiroyuki Matsumoto	ASAM.0041	4986
7590 03/07/2006				
REED SMITH LLP Suite 1400 3110 Fairview Park Drive Falls Church, VA 22042			EXAMINER NGUYEN, LUONG TRUNG	
			ART UNIT 2612	PAPER NUMBER

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/084,466

Applicant(s)

MATSUMOTO ET AL.

Examiner

LUONG T. NGUYEN

Art Unit

2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 December 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-6 and 12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6 is/are allowed.
- 6) ☒ Claim(s) 2-5 is/are rejected.
- 7) ☒ Claim(s) 12 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 12/27/2005 have been fully considered but they are not persuasive.

In re page 5, Applicants argue that Kasahara fails to teach or suggest such "first and second areas which are predetermined areas in a frame" as in the invention.

In response, regarding claim 2, Applicants amended claim 2 with limitations "the first area which is predetermined area in a frame," and "the second area which is a predetermined area in the frame." The Examiner considers that claim 2 as amended still does not distinguish from Kasahara et al. reference. Kasahara et al. discloses the unit area is preferred as a horizontal line (predetermined area, column 2, lines 30-55, column 8, lines 5-32) and unit area is also preferred as a plurality of adjacent horizontal lines (a predetermined area, column 2, lines 30-55, column 8, lines 5-32).

Claim Objections

2. Claim 3 is objected to because of the following informalities:

Claim 3, line 2, "judge means that" should be changed to --judge means judges that--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

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3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 2-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Kasahara et al. (U. S. Patent No. 6,710,818).

Regarding claim 2, Kasahara et al. discloses an imaging system including a solid-state CMOS imaging device and a signal processing semiconductor integrated circuit for processing read-out signals of pixels from said solid-state CMOS imaging device, comprising:

first level detection means which detects brightness on a first area (a horizontal line) set up on an imaging area of said solid-state CMOS imaging device, the first area which is predetermined area in a frame (the flicker judging circuit 5 judges whether illumination flicker exist in the video signal by frequency analyzing the dividing results of horizontal lines, Column 8, Lines 5-32, Column 2, Lines 30-55).

second level detection means which detects brightness on a second area (a plurality of horizontal lines) which is set up on an imaging area of said solid-state CMOS imaging device, and is larger than first area, the second area which is a predetermined area in the frame (the flicker judging circuit 5 judges whether illumination flicker exist in the video signal by frequency analyzing the dividing results of horizontal lines, Column 8, Lines 5-32, Column 2, Lines 30-55).

judgment means which judges turning-on-and-off of a light source illuminating (judging flicker) in accordance with an object to be imaged on the basis of detection levels of said first and second level detection means (the flicker judging circuit 5 judges whether illumination flicker exist in the video signal by frequency analyzing the dividing results of horizontal lines, Column 8, Lines 5-32, Column 2, Lines 30-55).

Regarding claim 3, Kasahara et al. discloses wherein said judgment means judges that said light source illuminating in accordance with the object is turned on and off when variation in the detection level of said first level detection means is larger than a predetermined level and variation in the detection level of said second level detection means is smaller than a second predetermined level (Column 9, Lines 1-67).

Regarding claim 4, Kasahara et al. discloses wherein said first area is constituted by pixels on a single horizontal scanning line (said unit area is a horizontal line, Column 2, Lines 50-55) and said second area is constituted by pixels on a plurality of horizontal scanning lines (said unit area is a plurality of horizontal lines, Column 2, Lines 50-55).

Regarding claim 5, Kasahara et al. discloses charge storage control means which sets up an electric charge storage time for each pixel of said solid-state CMOS imaging device to be equal to a turning-on-and-off period of said light source illuminating the object or an integral multiple thereof to thereby remove flicker (compensating flicker, Column 1, Lines 14-18, Column 2, Line 38-55).

Allowable Subject Matter

5. Claim 6 is allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 6, the prior art of the record fails to show or fairly suggest an imaging system including a solid-state CMOS imaging device and a signal processing semiconductor integrated circuit for processing read-out signals of pixels from said solid-state CMOS imaging device comprising wherein said judgment of the turning-on-and-off of said light source illuminating in accordance with the object on the basis of the detection levels of said first and second level detection means is performed by processing in accordance with the program in said control unit.

6. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 12, the prior art of the record fails to show or fairly suggest an imaging system including a solid-state CMOS imaging device and a signal processing semiconductor integrated circuit for processing read-out signals of pixels from said solid-state CMOS imaging device comprising wherein said judgment of the turning-on-and-off of said light source illuminating in accordance with the object on the basis of the detection levels of said first and second level detection means is performed by processing in accordance with the program in said control unit.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

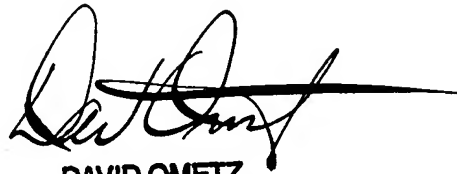
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID L. OMETZ can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LN LN
03/03/06

A handwritten signature in black ink, appearing to read 'David Ometz', with a long horizontal stroke extending to the right.

DAVID OMETZ
SUPERVISORY PATENT EXAMINER